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| 10/623,732 | 07/22/2003 | Kyoichi Suguro | 04329.2344-02 | 6071 |

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| EXAMINER | |
|---|---|
| LOKE, STEVEN HO YIN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/623,732 | SUGURO ET AL. | |
| | Examiner | Art Unit | |
| | Steven Loke | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-5 and 34-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 34-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "21" in fig. 4A. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The disclosure is objected to because of the following informalities: It is believed that the monocrystalline silicon substrate is "21" instead of "41" (page 32, line 3). It is believed that "76a" (not "15b") is being referred to the low concentration drain region (page 62, line 6). It is believed that "15b" (not "75b") is being referred to the high concentration source region (page 62, line 8). It is unclear what are the reference numerals for the projections and the isolating insulating film in figs. 19A to 19C.

Appropriate correction is required.

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The element isolating insulating film having a top surface

projecting upward above a surface of the semiconductor layer; and a MOS type element formed within said element region and having a gate insulating film and a metal gate electrode formed thereon, wherein: said gate insulating film and said metal gate electrode are formed on a top surface and sides of the semiconductor layer in said element region which are not covered with said element isolating insulating film as claimed in claim 3. The difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is at least five times as large as a thickness of said gate insulating film as claimed in claim 4. The MOS element includes a source/drain region and the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is substantially at least a junction depth of said source/drain region as claimed in claim 5. A metal gate electrode formed on the gate insulating film, said gate insulating film and said metal gate electrode being formed on a top surface and sides of the semiconductor layer in said element region which are not covered with said element isolating insulating film as claimed in claims 38 and 39.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the structures of claims 3-5, 38 and 39 as mentioned in paragraph 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. Claims 1, 2 and 39 are objected to because of the following informalities: Claim 1, line 8, the phrase "the element regions" has no antecedent basis. Claim 2, line 8, the phrase "said element regions" has no antecedent basis. Claim 39, line 2, the phrase "the gate insulating film" has no antecedent basis. Appropriate correction is required.

6. Claims 1-5 and 34-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 4-5, claim 2, lines 4-5, claim 3, lines 4-5, the phrase "an element isolating insulating film provided in the trench for partitioning said semiconductor layer into an element region" is vague and indefinite. Fig. 1E shows an element isolating

insulating film [2] provided in the trench for partitioning said semiconductor layer into a plurality of element regions. It is believed that the phrase should rewrite as "an element isolating insulating film provided in the trench for partitioning said semiconductor layer into a plurality of element regions".

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 2, 35 and 36 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yamazaki.

In regards to claim 1, Yamazaki shows all the elements of the claimed invention in fig. 8F. It is a semiconductor device, comprising: a substrate [101] having a semiconductor layer [103] and a trench (the area occupied by the lower portion of the oxide film [110]), said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions; an element isolating insulating film [110] provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a surface of said semiconductor layer; and a MOS type element formed within a corresponding one of the element regions and having a gate insulating film [118], wherein: a difference in height from the substrate between the top surface position of said element isolating insulating film and the top surface position of

said semiconductor layer is at least three times as large as the thickness of said gate insulating film.

In regards to claim 2, Yamazaki shows all the elements of the claimed invention in fig. 8F. It is a semiconductor device, comprising: a substrate [101] having a semiconductor layer [103] and a trench (the area occupied by the lower portion of the oxide film [110]), said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions; an element isolating insulating film [110] provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a surface of the semiconductor layer; and a MOS type element formed within a corresponding one of said element regions, wherein: a difference in height from the substrate between the top surface position of the semiconductor layer and the top surface position of the element isolating insulating film is at least 10 nm because the height of the top portion of the insulating film [110] is larger than the thickness of the gate insulating film [118] (col. 15, lines 10-14).

In regards to claims 35 and 36, Yamazaki further discloses said element isolating insulating film [110] is a thermally grown oxide film (LOCOS oxide film), and said element isolating insulating film and said element region make an interface which is substantially perpendicular to a top surface of said semiconductor layer [103].

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-5 and 34-39 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Dawson et al.

In regards to claim 1, Dawson et al. show all the elements of the claimed invention in figs. 2 and 4H. It is a semiconductor device, comprising: a substrate [10] having a semiconductor layer (col. 5, lines 8-10) and a trench (the area occupied by the lower portion of the dielectric film [5] and the dielectric film [80]), said semiconductor layer being an epitaxial layer (col. 5, lines 8-10), said trench partitioning said semiconductor layer into a plurality of regions; an element isolating insulating film [5, 80] provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a surface of said semiconductor layer; and a MOS type element formed within a corresponding one of the element regions and having a gate insulating film [86], wherein: a difference in height from the substrate between the top surface position of said element isolating insulating film [5, 80] and the top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film.

In regards to claim 2, Dawson et al. show all the elements of the claimed invention in figs. 2 and 4H. It is a semiconductor device, comprising: a substrate [10] having a semiconductor layer (col. 5, lines 8-10) and a trench (the area occupied by the lower portion of the dielectric film [5] and the dielectric film [80]), said semiconductor layer

being an epitaxial layer (col. 5, lines 8-10), said trench partitioning said semiconductor layer into a plurality of regions; an element isolating insulating film [5, 80] provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a surface of said semiconductor layer; and a MOS type element formed within a corresponding one of the element regions and having a gate insulating film [86], wherein: a difference in height from the substrate between the top surface position of said element isolating insulating film [5, 80] and the top surface position of said semiconductor layer is at least 10 nm (the thickness of the upper portion of the dielectric film [5] measured between the top surface of the dielectric film [5] and the top surface of the semiconductor layer is about 1050 nm).

In regards to claim 3, Dawson et al. show all the elements of the claimed invention in figs. 2 and 4H. It is a semiconductor device, comprising: a substrate [10] having a semiconductor layer (col. 5, lines 8-10) and a trench (the area occupied by the lower portion of the dielectric film [5] and the dielectric film [80]), said semiconductor layer being an epitaxial layer (col. 5, lines 8-10), said trench partitioning said semiconductor layer into a plurality of regions; an element isolating insulating film [5, 80] provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a surface of said semiconductor layer; and a MOS type element formed within said element region and having a gate insulating film [86] and a metal gate electrode [96] formed thereon, wherein: said gate insulating film and said metal gate electrode are formed on

a top surface and sides of the semiconductor layer in said element region which are not covered with said element isolating insulating film (see fig. 2).

In regards to claim 4, Dawson et al. further disclose the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is at least five times as large as a thickness of said gate insulating film.

In regards to claim 5, Dawson et al. further disclose the MOS element includes a source/drain region [94] and the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is substantially at least a junction depth of said source/drain region.

In regards to claim 34, Dawson et al. further disclose said element isolating insulating film [5, 80] and said gate insulating film [86] are formed in different steps.

In regards to claims 35-37, Dawson et al. further disclose said element isolating insulating film [5, 80] and said element region make an interface which is substantially perpendicular to a top surface of said semiconductor layer.

In regards to claims 35-37, the process limitation of how the element isolating insulating film is formed has no patentable weight in claim drawn to structure. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this

issue); and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Thus, the phrase "thermally grown" is thus non-limiting.

In regards to claims 38 and 39, Dawson et al. further disclose a metal gate electrode [96] formed on the gate insulating film [86], said gate insulating film and said metal gate electrode being formed on a top surface and sides of the semiconductor layer in said element region which are not covered with said element isolating insulating film (see fig. 2).

11. Applicant's arguments filed 9/7/04 have been fully considered but they are not persuasive.

It is urged, in page 15 of the remarks, that Yamazaki never discloses the trench and the element isolating insulating film as claimed in claims 1 and 2. However, the area occupied by the lower portion of the oxide film [110] in Yamazaki is considered as a trench and the oxide film [110] is considered as the element isolating insulating film. Therefore, Yamazaki does disclose the trench and the element isolating insulating film as claimed in claims 1 and 2.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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November 26, 2004

Steven Loke
Primary Examiner